FARADAY

FE 3010

AT PERIPHERAL CONTROL LOGIC

- **100% hardware and software compatible to the IBM PC-AT**
- **15 interrupt channels**
- **3 timer channels**
- **7 DMA channels**
- **TTL-compatible**
- **84-pin, J-type leaded surface mount plastic chip carrier**
- **8MHz DMA**
- **HCMOS technology**
- **256K or 1MB RAM chips**
- **DMA page registers**

Introduction

The Faraday FE3010 AT and peripheral controller is a highly integrated chip with various control and peripheral functions. The FE3010 replaces 21 IC components.

The FE3010 has been designed to enhance the IBM PC AT while being extremely flexible.

The FE3010 is used in conjunction with the Faraday FE3000, the PC AT CPU controller, the FE3020 address buffer, and the FE3030 data buffer to reduce the size of a typical PC AT motherboard by 80%, power by 70%, and the component count by 62%. The FE3010 has been designed to be upward-compatible with the Intel^{R} 80386 processor.

Figure 1 illustrates a block diagram of the FE3010 AT peripheral logic control integrated circuit. Refer to Table 1 for the pin descriptions shown in Figure 2.

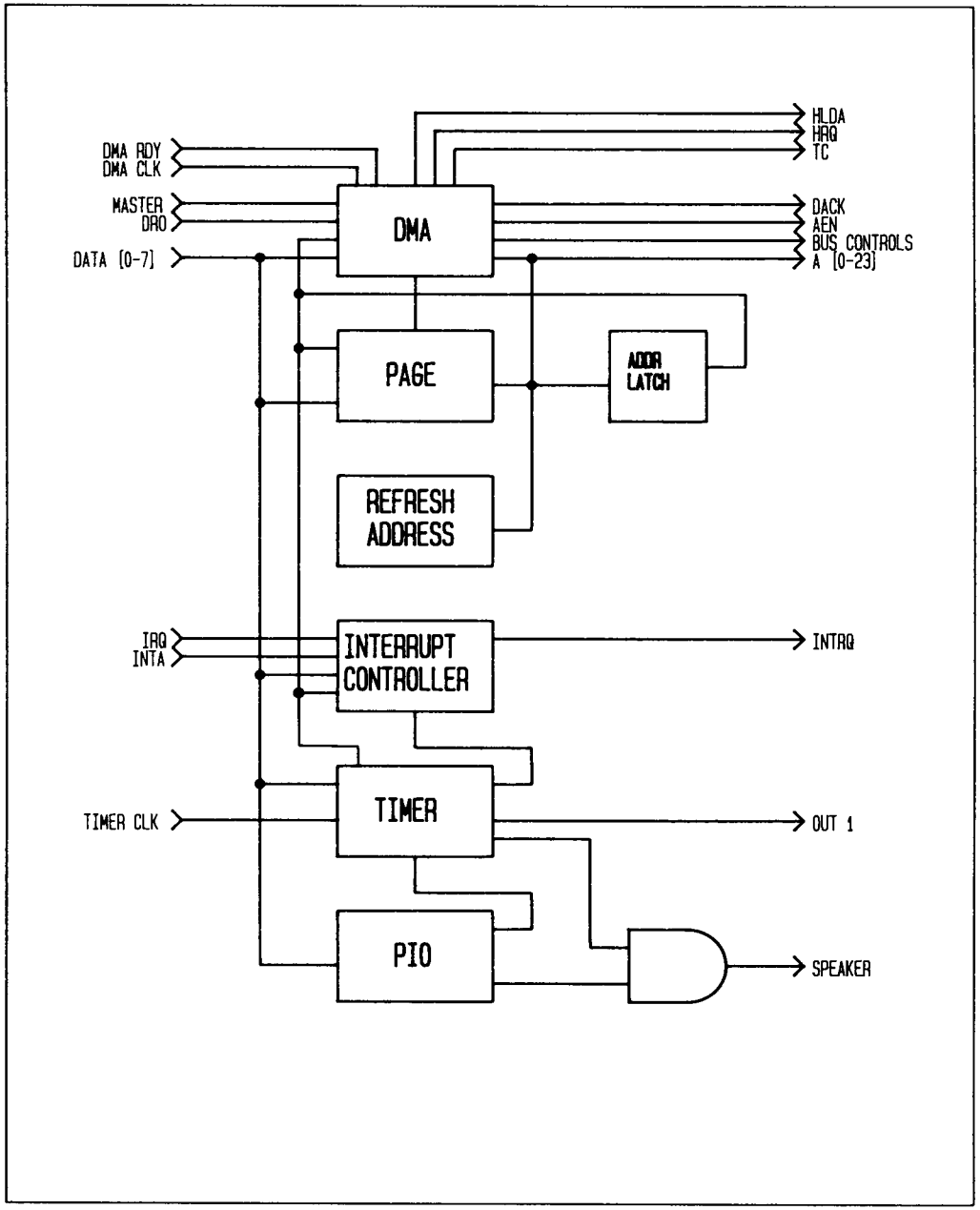

Figure 1. FE3010 Block Diagram

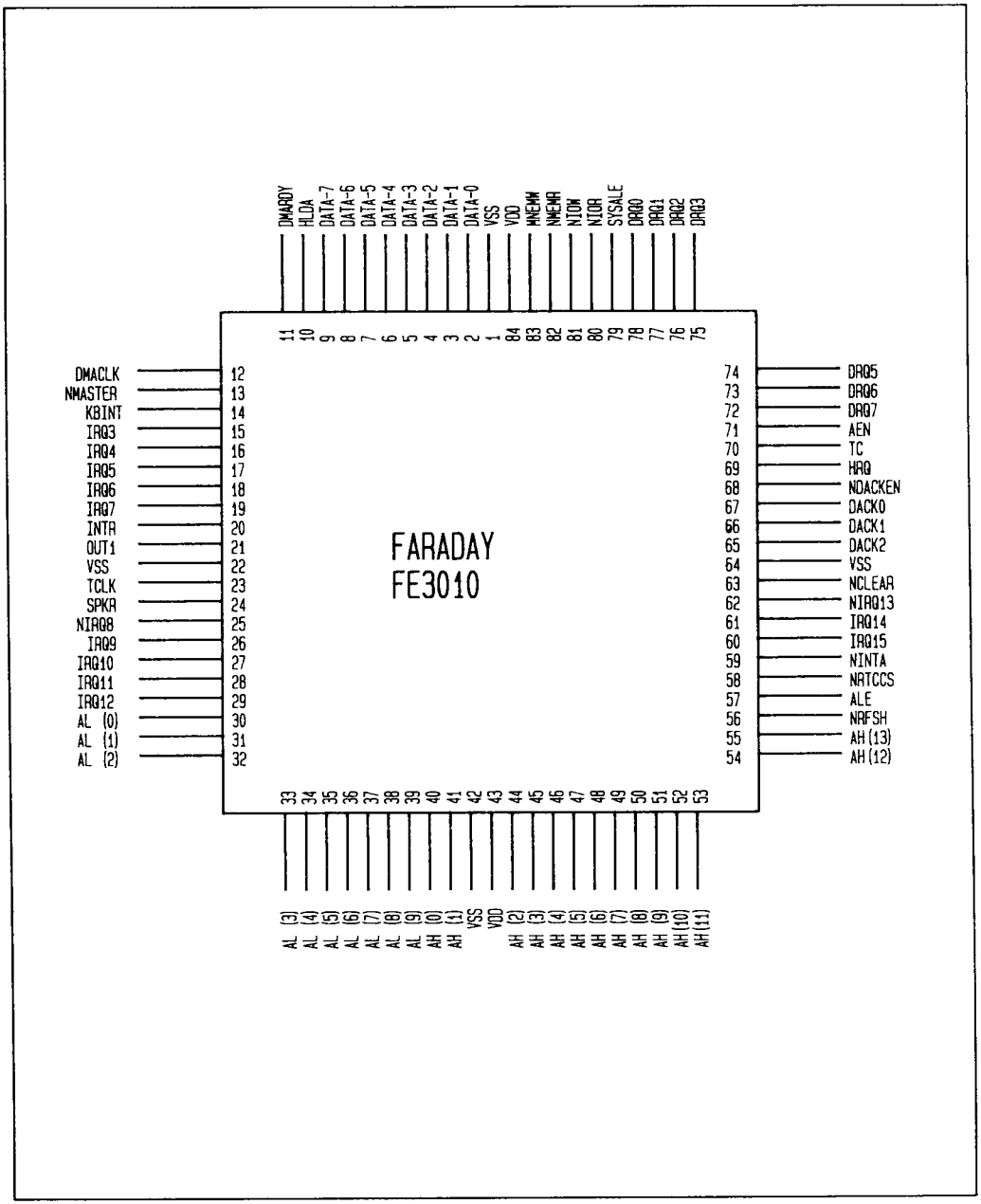

Figure 2. FE3010 Pin Diagram

Table 1. Pin Description

Pin	Type	Symbol	Function
1		V_{SS}	GROUND
2	I/O	DATA(0)	DATA BIT 0
3	I/O	DATA(1)	DATA BIT 1
4	I/O	DATA(2)	DATA BIT 2
5	I/O	DATA(3)	DATA BIT 3
6	I/O	DATA(4)	DATA BIT 4
7	I/O	DATA(5)	DATA BIT 5
8	I/O	DATA(6)	DATA BIT 6
9	I/O	DATA(7)	DATA BIT 7
10	I	HLDA	HOLD ACKNOWLEDGE Active high Acknowledge from the CPU (80286) for a request for the bus from the DMA controller.
11	I	DMARDY	DMA READY Active high Signal to indicate that the DMA may complete its current cycle.
12	I	DMACLK	DMA CLOCK System clock / DMACLK 6 MHz / 3 or 6 MHz 8 MHz / 4 or 8 MHz 10 MHz / 5 MHz
13	I	NMASTER	BUS MASTER Active low Signal to indicate that a master on the expansion bus has control of the bus.
14	I	KBINT	KEYBOARD INTERRUPT Active high
15	I	IRQ3	INTERRUPT REQUEST 3 Active high
16	I	IRQ4	INTERRUPT REQUEST 4 Active high
17	I	IRQ5	INTERRUPT REQUEST 5 Active high
18	I	IRQ6	INTERRUPT REQUEST 6 Active high
19	I	IRQ7	INTERRUPT REQUEST 7 Active high
20	O	INTR	INTERRUPT REQUEST TO CPU (80286) Active high
21	O	OUT 1	TIMER CHANNEL 1 OUTPUT
22		V_{SS}	GROUND

Table 1. Pin Description *(cont'd)*

Pin	Type	Symbol	Function
23	I	TCLK	TIMER CLOCK (1.19 MHz clock for timer)
24	O	SPKR	SPEAKER
25	I	NIRQ8	INTERRUPT REQUEST 8 Active low
26	I	IRQ9	INTERRUPT REQUEST 9 Active high
27	I	IRQ10	INTERRUPT REQUEST 10 Active high
28	I	IRQ11	INTERRUPT REQUEST 11 Active high
29	I	IRQ12	INTERRUPT REQUEST 12 Active high
30	I/O	AL(0)	ADDRESS BIT 0
31	I/O	AL(1)	ADDRESS BIT 1
32	I/O	AL(2)	ADDRESS BIT 2
33	I/O	AL(3)	ADDRESS BIT 3
34	I/O	AL(4)	ADDRESS BIT 4
35	I/O	AL(5)	ADDRESS BIT 5
36	I/O	AL(6)	ADDRESS BIT 6
37	I/O	AL(7)	ADDRESS BIT 7
38	I/O	AL(8)	ADDRESS BIT 8
39	I/O	AL(9)	ADDRESS BIT 9
40	O	AH(0)	ADDRESS BIT 10
41	O	AH(1)	ADDRESS BIT 11
42		V_{SS}	GROUND
43		V_{DD}	+5 VOLTS SUPPLY
44	O	AH(2)	ADDRESS BIT 12
45	O	AH(3)	ADDRESS BIT 13
46	O	AH(4)	ADDRESS BIT 14
47	O	AH(5)	ADDRESS BIT 15
48	O	AH(6)	ADDRESS BIT 16
49	O	AH(7)	ADDRESS BIT 17
50	O	AH(8)	ADDRESS BIT 18
51	O	AH(9)	ADDRESS BIT 19
52	O	AH(10)	ADDRESS BIT 20

Table 1. Pin Description *(cont'd)*

Pin	Type	Symbol	Function
53	O	AH(11)	ADDRESS BIT 21
54	O	AH(12)	ADDRESS BIT 22
55	O	AH(13)	ADDRESS BIT 23
56	I	NRFSH	REFRESH ADDRESS Active low Signal to enable the refresh address to the address bus during a RAM refresh cycle.
57	I	ALE	ADDRESS LATCH ENABLE Active high
58	O	NRTCCS	REAL TIME CLOCK CHIP SELECT Active low
59	I	NINTA	INTERRUPT ACKNOWLEDGE FROM CPU (80286) Active low Interrupt acknowledge to the interrupt controllers.
60	I	IRQ15	INTERRUPT REQUEST 15 Active high
61	I	IRQ14	INTERRUPT REQUEST 14 Active high
62	I	NIRQ13	INTERRUPT REQUEST 13 Active low Error interrupt from (80287).
63	I	NCLEAR	SYSTEM CLEAR Active low
64		V_{SS}	GROUND
65	O	DACK2	DMA ACKNOWLEDGE BIT 2
66	O	DACK1	DMA ACKNOWLEDGE BIT 1
67	O	DACK0	DMA ACKNOWLEDGE BIT 0
68	O	NDACKEN	DMA ACKNOWLEDGE ENABLE Active low Signal to enable DACK0, DACK1, and DACK2 decodes.

DACK2	DACK1	DACK0	DMA Channel Acknowledge
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	Illegal
1	0	1	5
1	1	0	6
1	1	1	7

Table 1. Pin Description *(cont'd)*

Pin	Type	Symbol	Function
69	O	HRQ	DMA REQUEST TO CPU (80286) Active high
70	O	TC	DMA END OF OPERATION Active high Signal to indicate the DMA controller has finished its cycle.
71	O	AEN	DMA AEN Active high Signal to indicate that the current bus is a DMA cycle.
72	I	DRQ7	CHANNEL 7 DMA REQUEST Active high
73	I	DRQ6	CHANNEL 6 DMA REQUEST Active high
74	I	DRQ5	CHANNEL 5 DMA REQUEST Active high
75	I	DRQ3	CHANNEL 3 DMA REQUEST Active high
76	I	DRQ2	CHANNEL 2 DMA REQUEST Active high
77	I	DRQ1	CHANNEL 1 DMA REQUEST Active high
78	I	DRQ0	CHANNEL 0 DMA REQUEST Active high
79	O	SYSALE	SYSTEM ALE Active high Signal to latch the address in the address latch.
80	I/O	NIOR	I/O READ COMMAND Active low
81	I/O	NIOW	I/O WRITE COMMAND Active low
82	O	NMEMR	MEMORY READ COMMAND Active low
83	O	NMEMW	MEMORY WRITE COMMAND Active low
84		V_{DD}	+5 VOLTS SUPPLY

FUNCTIONAL DESCRIPTION

DMA

This block contains the functional equivalent of two 8237 DMA controllers in cascade mode. This block improves the microprocessor's system by allowing external devices to transfer information directly from the system memory.

Features:

- o Address increment or decrement.
- o Seven independent DMA channels.
- o Independent auto-initialization of all channels.
- o Enable/disable control of individual DMA request.
- o Software DMA request.

Page

The page register is an 8-bit by 16-byte dual-ported RAM. It is used to generate address bits 16 to 23 for 8-bit DMA transfers and address bits 17 to 23 for 16-bit DMA transfers, and refresh cycles. One port of the RAM is a read-only port for DMA or refresh cycles, and the other is a read/write port for the 80286 CPU.

Interrupt Controller

This block contains the functional equivalent to two 8259 interrupt controllers in cascade mode. A total of 15 interrupts are supported including one from the timer block.

Timer

The timer is the functional equivalent of an 8254 timer. One channel is used to generate refresh requests, one is used to generate sound for the speaker, and the other is tied to interrupt 0.

PIO

This block contains a control port to control the speaker and timer channel. It also contains circuitry to detect if refresh is running. This condition may be read back as bit 4. Bits 2 and 3 are read/write, but they do not perform any function. They are used for software compatibility with the IBM PC AT.

Refresh Address

This block contains a 9-bit counter that is used for the address during a refresh.

Table 2. Absolute Maximum Ratings*

T_A = +25 ° C

Power supply voltage, V_{DD} @ V_{SS}=0	3.0 V to +7.0 V
Power dissipation, PDMAX @V_{DD}=5.25V	200mW
Current, I_{DD} @V_{DD}=5.25V	38mA
Input voltage, VI	0.0V to V_{DD} + 0.3V
Output voltage, VO	0.0 V to V_{DD} + 0.3V
Operating temperature, TOPT	0 ° C TO +70 ° C
Storage temperature, TSTG	-40 ° C to +125 ° C

*Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Capacitance

T_A = +25 ° C, V_{DD} = 0V

		Limits			
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Test Condition**
Input capacitance	C_I		10	pF	fc = 1 MHz unmeasured pins
I/O capacitance	C_{IO}		15	pF	returned to 0V

Table 4. DC Characteristics

T_A = 0 ° C to +70 ° C, V_{DD} = +5V ± 5%

[ALE, DMACLK, DMARDY, DRQ0, DRQ1, DRQ2, DRQ3, DRQ5, DRQ6, DRQ7, HLDA, IRQ3, IRQ4, IRQ5, IRQ6, IRQ7, IRQ9, IRQ10, IRQ11, IRQ12, IRQ14, IRQ15, KBINT, NCLEAR, NINTA, NIRQ13, NMASTER, NRFSH, TLCK, NIRQ8]

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	V_{IL}	V_{SS}	0.8	V	V_{DD} = 5V ± 5%
Input high voltage	V_{IH}	2.0	V_{DD}	V	V_{DD} = 5V ± 5%
Input low current	I_{IL}	-10.0	-300.0	uA	V_{IN} = 0.0V
Input high current	I_{IH}		40.0	uA	V_{IN} = V_{DD}

[A(0), A(1), A(2), A(3), A(4), A(5), A(6), A(7), A(8), A(9), DATA(0), DATA(1), DATA(2), DATA(3), DATA (4) DATA(5), DATA(6), DATA(7), NIOR, NIOW]

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	V_{IL}	V_{SS}	O.8	V	V_{DD} = 5V ± 5%
Input high voltage	V_{IH}	2.0	V_{DD}	V	V_{DD} = 5V ± 5%
Input low current	I_{IL}		-10.0	uA	V_{IN} = 0.0V
Input high current	I_{IH}		10.0	uA	V_{IN} = V_{DD}
Output low voltage	V_{OL}		0.4	V	I_{OL} = 4.0mA
Output high voltage	V_{OH}	2.4		V	I_{OH} = -4.0mA
Output current	IOZ	-10.0	10.0	uA	0V < V_{OUT} < V_{DD}

Table 4. DC Characteristics *(cont'd)*

T_A = 0 ° C to +70 ° C, V_{DD} = +5V ± 5%

[AEN, DACK0, DACK1, DACK2, HRQ, INTR, NDACKEN, NRTCCS, OUT1, SPKR, SYSALE, TC]

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	V_{OL}		0.4	V	I_{OL} = 2.0mA
Output high voltage	V_{OH}	2.4		V	I_{OH} = -2.4mA

[A(10), A(11), A(12), A(13), A(14), A(15), A16), A(17), A(18), A(19), A(20), A(21), A(22), A(23), NMEMR, NMEMW]

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	V_{OL}		0.4	V	I_{OL} = 4.0mA
Output high voltage	V_{OH}	2.4		V	I_{OH} = -4.0mA
Output current	IOZ	-10.0	10.0	uA	$0V < V_{OUT} < V_{DD}$

Table 5. AC Characteristics

TA = 0 ° C to +70 ° C, V_{DD} = +5V ± 5%, load capacitance=85pF, operating at 8MHz.

Symbol	Parameter	Min	Typ	Max	Unit
t1	DRQ high setup time to DMACLK high.	3	-2	-7	ns
t2	HRQ active high delay from DMACLK rising edge.	10	28	49	ns
t3	DMACLK high setup time delay from HLDA rising edge.	-2	1	4	ns
t4	AEN active high delay from DMACLK falling edge.	14	40	69	ns
t5	AEN inactive low delay from DMACLK rising edge.	15	43	74	ns
t6	SYSALE active high delay from DMACLK rising edge.	10	29	50	ns
t7	SYSALE inactive low delay from DMACLK rising edge.	14	40	69	ns
t8	NIOR and NMEMR active low delay from DMACLK rising edge.	12	34	60	ns
t9	NIOW and NMEMW active low delay from DMACLK rising edge.	12	34	60	ns
t10	NIOR and NMEMR inactive high delay from DMACLK rising edge.	11	30	52	ns
t11	NIOW and NMEMW inactive high delay from DMACLK rising edge.	11	30	52	ns
t12	NDACKEN active low delay from DMACLK falling edge.	13	37	63	ns
t13	NDACKEN inactive high delay from DMACLK falling edge.	10	28	49	ns
t14	TC active high delay from DMACLK falling edge.	11	32	56	ns
t15	TC inactive low delay from DMACLK falling edge.	13	39	68	ns
t16	DMARDY high setup time delay to DMACLK rising edge.	-13	-5	2	ns
t17	ADDR active delay from AEN rising edge.	2	10	18	ns

Table 5. AC Characteristics *(cont'd)*
TA = 0 ° C to +70 ° C, V_{DD} = +5V ± 5%, load capacitance=85pF, operating at 8MHz.

Symbol	Parameter	Min	Typ	Max	Unit
t18	ADDR valid delay from AEN rising edge.	70	89	109	ns
t19	ADDR float delay from AEN falling edge.	1	5	9	ns
t20	DATA valid delay from NIOR falling edge.	14	39	68	ns
t21	DATA float delay from NIOR rising edge.	11	30	51	ns
t22	ADDR valid setup time to SYSALE inactive low.	71	92	111	ns
t23	SYSALE inactive low to ADDR valid hold time.	121	123	124	ns
t24	ADDR valid delay from NRFSH falling edge.	15	45	78	ns
t25	ADDR float delay from NRFSH rising edge.	10	30	60	ns
t26	SYSALE active high from delay NFRSH falling edge.	6	17	29	ns
t27	SYSALE inactive low delay from NRFSH rising edge.	8	6	40	ns
t28	SYSALE active high delay from ALE rising edge.	5	16	27	ns
t29	SYSALE inactive low delay from ALE falling edge.	9	26	46	ns
t30	INTR (master) active high delay from IRQ rising edge.	11	32	55	ns
t31	INTR (slave) active high from ALE rising edge.	27	74	129	ns
t32	DATA valid delay from NINTA falling edge.	17	49	84	ns
t33	DATA float delay from NINTA rising edge.	9	26	45	ns
t34	NRTCCS active low delay from ALE rising edge.	13	38	66	ns
t35	NRTCCS inactive high delay from ALE rising edge.	9	27	46	ns

Table 5. AC Characteristics *(cont'd)*

TA = 0 ° C to +70 ° C, V_{DD} = +5V ± 5%, load capacitance=85pF, operating at 8MHz.

Symbol	Parameter	Min	Typ	Max	Unit
t36	OUT1 active high delay from TCLK falling edge.	7	20	35	ns
t37	OUT1 inactive low delay from TCLK falling edge.	10	29	51	ns
t38	DATA invalid time delay from DATA to NIOW inactive high.	9	18	28	ns

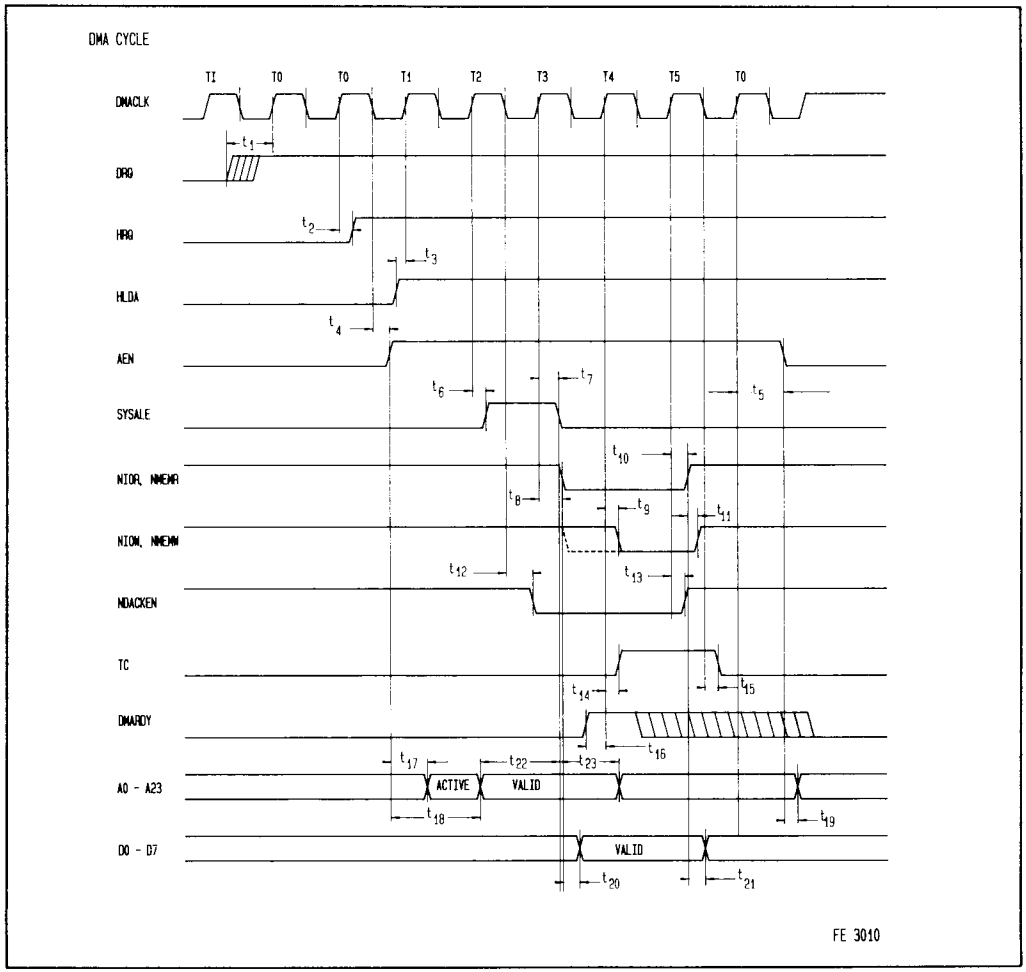

Figure 3. DMA Cycle

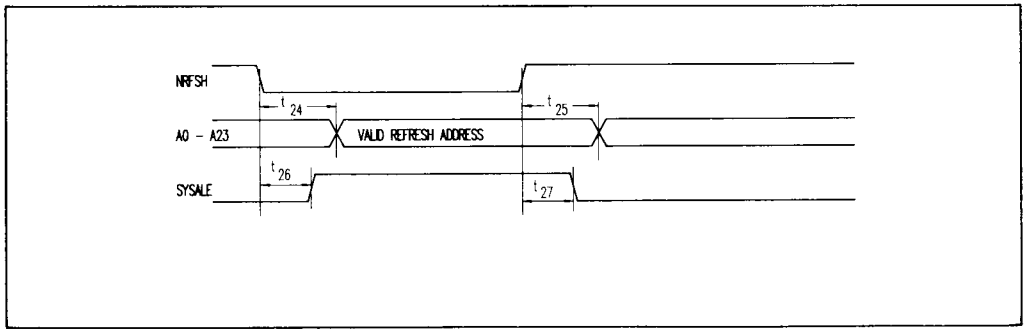

Figure 4. Refresh Cycle

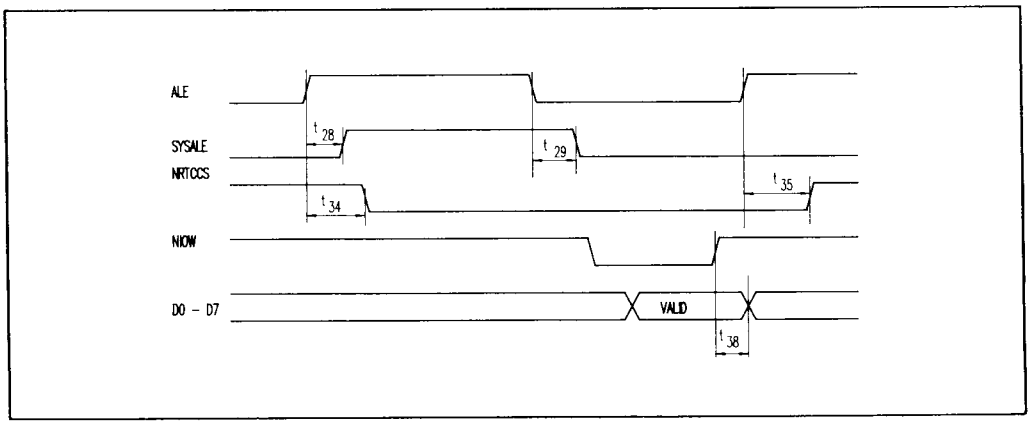

Figure 5. CPU Cycle

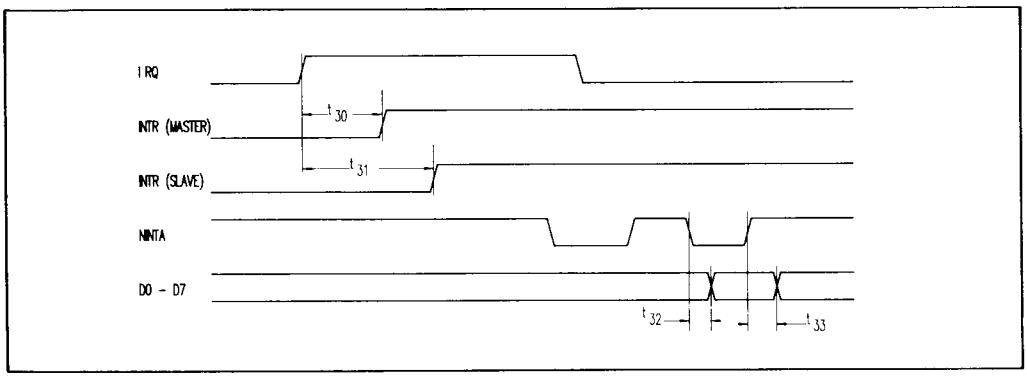

Figure 6. Interrupt Cycle

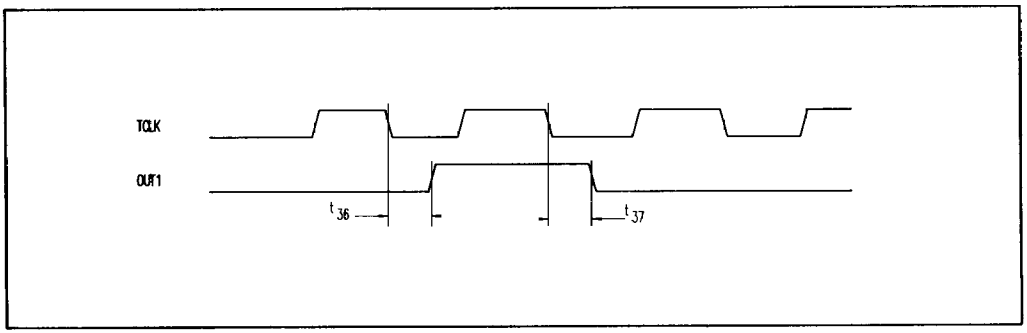

Figure 7. Timer Cycle

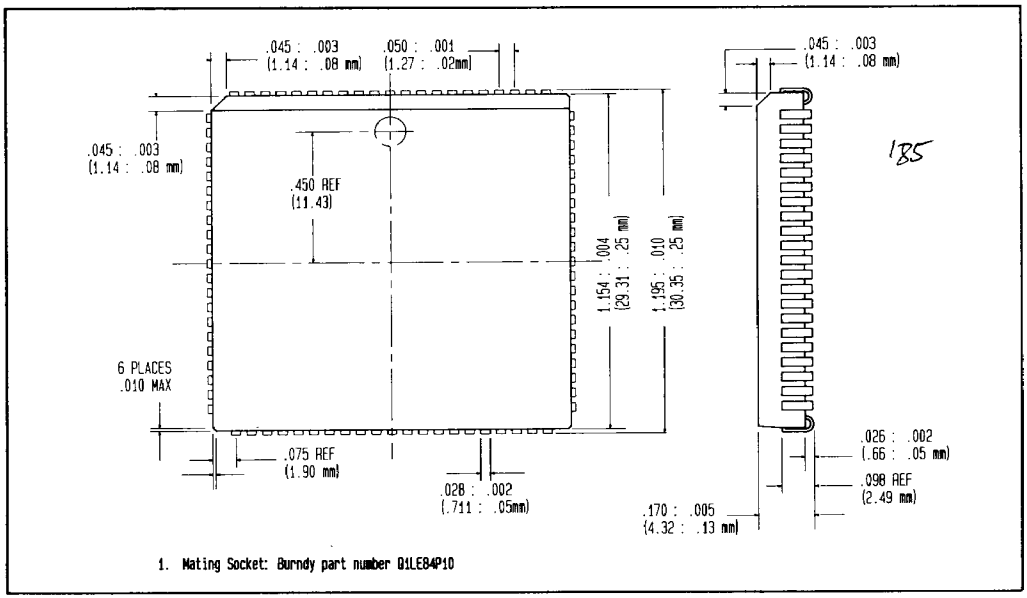

Figure 8. FE3010 84-Pin Plastic Chip Carrier (J-Bend Leads)